A System and Method for Reducing Leakage in Memory Cells Using Wordline Control

FIELD OF THE INVENTION

[001] This invention relates generally to electronic circuits. More particularly, this invention relates to reducing average power in memory cells.

BACKGROUND OF THE INVENTION

[002] As more electronic circuits are included on a single die, the power dissipated by a single die continues to increase. In order to keep a single IC (integrated circuit) at a reasonable temperature, many techniques have been used. For example, elaborate cooling fins have been attached to the substrate of ICs. Also, fans have been positioned near a group of IC's to cool them. In some cases, liquids have been used to remove the heat produced by ICs. These solutions can be costly and may require a great deal of space, where space is at a premium. If the power on ICs can be reduced while still achieving higher levels of integration, the cost and area of devices that use ICs may be reduced.

[003] The number of bits contained on a semiconductor memory chip, has, on average, quadrupled every three years. As a result, the power that semiconductor memories consume has increased. Computer systems may use large numbers of stand-alone semiconductor memories. Part of the semiconductor memory used by these computer systems may be held in standby mode for a certain amount of time. The portion of memory that is held in standby is not accessed for data and as result, has lower power requirements than those parts of semiconductor memory that are accessed.

[004] Part of the power used in stand-by mode is created by subthreshold and gate leakage currents in each individual memory cell of the semiconductor memory. Because the amount of memory used in a computer system or as part of a microprocessor chip is increasing, the power, as result of leakage currents in semiconductor memory cells is also increasing. Typically, leakage is proportional to the voltage applied to a memory cell.

[005] Several methods have been used to reduce subthreshold leakage in memory cells. One method increases the V_t of the transistors in the memory cell. Another method increases the thickness of the gate oxide of the transistors in the memory cell. These methods typically require extra processing steps. These extra processing steps increase the cost of an IC. In addition these methods may reduce the speed at which data may be accessed from the memory cells.

[006] Another method for reducing power used by memory cells is to provide a separate lower voltage power supply for memory cells. This method requires a more complex package for an IC and more design effort to physically route another power supply. As result, the cost of a packaged IC typically increases.

[007] There is a need in the art to reduce the power consumed by memory cells. An embodiment of this invention reduces the power used by memory cells without significantly increasing the cost of a packaged IC or without significantly increasing the data access times of the memory cells.

SUMMARY OF THE INVENTION

[008] An embodiment of the invention provides a circuit for reducing power in memory cells. The input of the circuit is connected to a wordline of the memory cells.

When the wordline is active, the output of the circuit applies a voltage near VDD to the positive voltage supply node of the memory cells. When the wordline is inactive, the output of the circuit applies a voltage that is reduced by at least one V_t from VDD to the positive voltage supply node of the memory cells.

[009] Other aspects and advantages of the present invention will become apparent from the following detailed description, taken in conjunction with the accompanying drawings, illustrating by way of example the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[010] Figure 1 is a schematic drawing of a 6 transistor SRAM cell. Prior Art

[011] Figure 2 is a block diagram of a memory array with 128 wordlines with 32 memory cells on each wordline. Prior Art

[012] Figure 3 is a block diagram of a memory array with 128 wordlines with 32 memory cells on each wordline using an embodiment of the invention.

[013] Figure 4 is a schematic drawing of a first embodiment of the invention.

[014] Figure 5 is a schematic drawing of a second embodiment of the invention.

[015] Figure 6 is a schematic drawing of a third embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[016] Figure 1 is a schematic drawing of a 6 transistor SRAM cell. This memory cell is used as an example of a memory cell that may be used with an embodiment of the invention to reduce power in memory arrays. Other memory cells may be used with other embodiments of the invention to reduce power in memory arrays.

[017] In Figure 1, the sources, of PFETs (P-type Field Effect Transistor) **MP1, 112**, and **MP2, 114** are connected to positive power supply, **VDD**. The drain of PFET, **MP1, 112**, the drain of NFET (N-type Field Effect Transistor), **MN1, 116**, the drain of NFET, **MN3, 120**, the gate of PFET, **MP2, 114** and the gate of NFET, **MN2, 118** are connected to node **108**. The sources of NFETs, **MN1, 116**, and **MN2, 118**, are connected to **GND**. The drain of PFET, **MP2, 114**, the drain of NFET, **MN2, 118**, the drain of NFET, **MN4, 122**, the gate of PFET, **MP1, 112**, and the gate of NFET, **MN1, 116**, are connected to node **110**. The gates of NFETs, **MN3, 120**, and **MN4, 122** are connected to wordline, **WL1, 104**. Bitline, **BL1, 100** is connected to the source of NFET, **MN3, 120**. Bitline, **BL2, 102** is connected to the source of NFET, **MN4, 122**.

[018] Data is typically read from the SRAM cell in Figure 1 by applying a logical "one" on **WL1, 104**. **BL1, 100**, and **BL2, 102**, are typically pre-charged to a voltage at or near VDD, before the data is read from the SRAM cell. One of the bitlines, **BL1, 100**, or **BL2, 102**, is discharged to a voltage lower than the precharge voltage while the other bitline remains near its precharged value when the SRAM cell is read. The differential voltage between **BL1, 100** and **BL2, 102**, is usually detected

by a sense-amp and the sense-amp outputs a logical one or zero depending on the differential voltage on the bitlines, **BL1, 100**, and **BL2, 102**.

[019] Writing the SRAM cell in Figure 1 is typically achieved by applying a logical high value on one bitline and a logical low value on the other bitline while driving the wordline, **WL1, 104**, to a high value. The logical value on **BL1, 100**, is forced on the node, **108**, of the SRAM cell, while the opposite logical value on **BL2, 102**, is forced on the node **110** of the SRAM cell.

[020] Figure 2 is a block diagram of a memory array with 128 wordlines with 32 memory cells on each wordline. The strap cell, **200**, shown in Figure 2, does nothing from a logical perspective but it used to implement the physical layout of the memory array.

[021] For area efficiency, memory cells are typically small enough to where they don't have room to contact the wordlines from the higher metal layers into each cell. The strap cell, **200**, provides this function. For example, a metal line wordline, **234**, connects to a poly-silicon wordline, **WL1, 202**. The poly-silicon wordline, **WL1, 202**, makes connections to the appropriate transistors in memory cells, **MC1/1** through **MC1/32**. Metal wordlines, **236, 238**, and **240** provide connections to poly-silicon wordlines, **WL2, 204, WL127, 206**, and **WL128, 208** respectively. In Figure 2, the positive supply voltage, **VDD**, is applied to all the memory cells. **VDD**, in this example, is designed to remain a constant voltage.

[022] Figure 3 is a block diagram of a memory array with 128 wordlines with 32 memory cells on each wordline using an embodiment of the invention. The strap cell, **300**, shown in Figure 3, in addition to providing a method to connect metal wordlines to poly-silicon wordlines, contains an embodiment of the invention.

For example, in Figure 3, metal wordline, **350**, is connected to poly-silicon worldine, **WL1**, **302**. In addition, wordline, **WL1**, **350**, is an input to an embodiment of the invention, **342**. The output of an embodiment of the invention, **342**, is connected to the positive voltage supply node, **334** of the memory cells, **MC1/1** through **MC1/32**. When the wordline, **350**, is driven to a high logical value, the output of an embodiment of the invention, **342**, provides a voltage near **VDD** to the positive voltage supply node **334**.

[023] When the wordline, **350**, is driven to a low logical value, the output of an embodiment of the invention, **342**, provides a voltage at least one V_t below **VDD** to the positive voltage supply node **334**. When the voltage applied to positive supply node **334** is reduced, the power consumed by memory cells, **MC1/1** through **MC1/32** is reduced.

[024] Figure 4 is a schematic drawing of a first embodiment of the invention. A wordline, **WL**, for example, is connected to the input, **400**, of inverter, **INV1**. The output, **402**, of inverter, **INV1**, is connected to the gate, **402**, of PFET, **PFET1**. The source of **PFET1**, the drain of **NFET1**, and the gate of **NFET1** are connected to **VDD**. The drain, **406**, of **PFET1**, and the source, **406**, of **NFET1**, are connected to a positive voltage supply node, **PVSN**, of a group of memory cells.

[025] In Figure 4, when the **WL**, **400**, goes to a high logical value, the output, **402**, of the inverter, **INV1**, goes low. A low logical value on the gate of **PFET1** causes **PFET1** to turn on and transfers a voltage close to **VDD** to the positive voltage supply node, **PVSN**, **406**. When **WL**, **400**, goes to a low logical value, the output, **402**, of inverter, **INV1**, goes to a high logical value. A high logical value on the gate of **PFET1**, cause **PFET1** to turn off. **NFET1** is configured as diode and as

consequence of the leakage of the memory cells supplied by **PVSN**, the voltage on the positive voltage supply node, **PVSN, 406** droops to near VDD-V_t.

[026] Figure 5 is a schematic drawing of a second embodiment of the invention. In this embodiment, an active-low wordline, **WLN, 500**, is connected to the input of an inverter, **INV1**, and to the gate of **PFET1**. The output, **502**, of the inverter, **INV1** is connected to a local wordline, **WL**. The source of **PFET1**, the drain of **NFET1**, and the gate of **NFET1** are connected to **VDD**. The drain of **PFET1** and the source of **NFET1** are connected to a positive voltage supply node, **PVSN, 504**, of a group of memory cells.

[027] In Figure 5, when the active-low wordline, **WLN, 500**, goes to a low logical value, the output, **502**, local wordline **WL**, of the inverter, **INV1**, goes high. A low logical value on the gate of **PFET1** causes **PFET1** to turn on and transfers a voltage close to **VDD** to the positive voltage supply node, **PVSN, 504**. When the active-low wordline, **WLN, 500**, goes to a high logical value, the local wordline **WL, 502**, of inverter, **INV1**, goes to a low logical value. A high logical value on the gate of **PFET1**, cause **PFET1** to turn off. **NFET1** is configured as diode and as consequence of the leakage of the memory cells supplied by **PVSN**, the voltage on the positive voltage supply node, **PVSN, 504**, droops to near VDD-V_t.

[028] Figure 6 is a schematic drawing of a third embodiment of the invention. In this embodiment, **WL, 600**, is connected to the gate of **NFET1**. The drain of **NFET1**, the source of **NFET1**, and the source of **NFET2** are connected to the gate of **NFET3**. The drain of **NFET2**, the drain of **NFET3**, the drain of **NFET4**, the gate of **NFET2**, and the gate of **NFET4** are connected to **VDD**. The source of **NFET3** and the source of **NFET4** are connected to positive voltage supply node, **PVSN, 604**.

[029] In Figure 6, when **WL, 600**, goes high, it boot-straps the voltage on node **602** above **VDD**. Since the voltage on the gate of **NFET3** is high enough above **VDD, VDD** may be transferred to the positive voltage supply node, **PVSN, 604**. When **WL, 600**, goes low, the voltage on node **602** is not high enough to turn **NFET3** on. **NFET4** is configured as diode and as consequence of the leakage of the memory cells supplied by **PVSN**, the voltage on the positive voltage supply node, **PVSN, 604**, droops to near VDD-V_t.

[030] The foregoing description of the present invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed, and other modifications and variations may be possible in light of the above teachings. The embodiment was chosen and described in order to best explain the principles of the invention and its practical application to thereby enable others skilled in the art to best utilize the invention in various embodiments and various modifications as are suited to the particular use contemplated. It is intended that the appended claims be construed to include other alternative embodiments of the invention except insofar as limited by the prior art.